REMARKS

Claims 1-30 were pending in the above-identified application and stand rejected. Applicants respectfully request reconsideration.

Rejections Under 35 U.S.C. §112

Claims 1-30 stand rejected under 35 U.S.C. §112, first paragraph, as failing to comply with the enablement requirement. Specifically, the Examiner states:

> In claims 1, 9, 15 and 22, the limitations "signal envelope voltage", "clock envelope voltage" and "group envelope voltage" are recited. However, the specification does not explain the natures of the signal envelope voltage, clock envelope voltage and group envelope voltage. Without some disclosure as to what constitutes the signal envelope voltage, clock envelope voltage and group envelope voltage, *one skilled in the art not [sic] be able to make and use the signal envelope voltage, clock envelope voltage and group envelope voltage.*

(OA, page 23, paragraph 4, emphasis added.) In summary, based upon the emphasized language in the foregoing quote, applicants understand the examiner to be arguing that those of skill in the art would not be able to make and use the three types of "envelope voltages" recited in the claims. Applicants respectfully disagree.

Applicants direct the Examiner's attention to MPEP 2164.01, which summarizes the test for enablement. Summarized even further here, for brevity, the enablement requirement "has been interpreted to require that the claimed invention be enabled so that any person skilled in the art can make and use the invention without undue experimentation." (MPEP 2164.01., citing In re Wands, 858 F.2d at 737, 8 USPQ2d at 1404 (Fed. Cir. 1988)).

The examiner bears the initial burden of establishing a reasonable basis to question enablement (MPEP 2164.04). MPEP 2164.01 lists a number of specific factors to consider in determining whether experimentation is "undue," and further remarks that "if an enablement rejection is appropriate, the first Office action on the merits should present the best case *with all the relevant reasons, issues, and evidence....*" (MPEP 2164.04, emphasis added). The examiner did not address *any* of the relevant factors, and so has failed to meet this burden. The rejection of

claims 1-30 for failure to enable should therefore be withdrawn.

Despite the lack of support for the enablement rejections, Applicants address each of the examiner's concerns by pointing to specific support for each of the three "envelope voltages" recited in the claims and subject to the enablement rejections.

Signal Envelope Voltage

Applicants' specification introduces a "signal envelope voltage" in connection with Fig. 4. Applicants note, for example:

> The automatic gain control is implemented in part by signal envelope detection circuitry 44 that is responsive to the amplified data output signal D_{OUT} to indicate an amplified **signal envelope voltage VO_{ENV}**. VO_{ENV} tracks the voltage swing or peak voltage of D_{OUT}.

(Spec., page 8, lines 2-5, emphasis added.) The emphasized language refers to the signal envelope voltage, which is abbreviated VO_{ENV} in Fig. 4 and elsewhere. Fig. 4, reproduced below, clearly shows the "signal envelope detection circuitry 44" of the quote, including the node that provides the "signal envelope voltage VO_{ENV}" in support of the identical claim language. Fig. 4, and the corresponding text, shows how to "use" a signal envelope voltage in accordance with one embodiment.

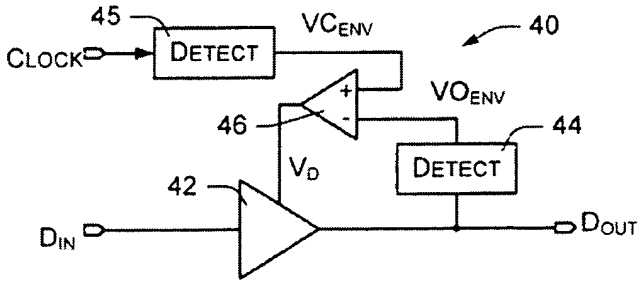

Fig. 4

In the sentence immediately following the last quote, applicants' specification remarks that "Fig. 2 shows a simplified example of an appropriate envelope detector" (*Id.* at lines 5 and 6). That is

to say, detector 44 of Fig. 4 can be implemented using the circuit of Fig. 2, a conventional envelope detector. Fig. 2 is reproduced below.

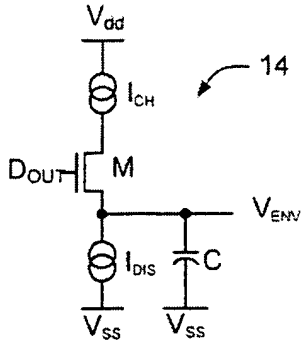

Fig. 2
Prior Art

Fig. 2 and the associated text show how to "make" a signal envelope voltage for use in some embodiments, including the embodiment of Fig. 4. Applicants' specification thus fully describes and schematically details circuits for making (Fig. 2) and using (Fig. 4) a "signal envelope voltage" in support of the claims. This is ample direction for those familiar with gain control and signal receivers. The rejections of the claims for failing to enable a "signal envelope voltage" should therefore be withdrawn.

Clock Envelope Voltage

Applicants' specification references a "clock envelope voltage" many times, first introducing this claim element in connection with the same Fig. 4 reproduced above.

> The automatic gain control of circuit 40 also comprises clock envelope detection circuitry 45 responsive to clock signal CLOCK to indicate **a clock envelope voltage VC_{ENV}**. VC_{ENV} tracks the voltage swing or peak voltage of clock signal CLOCK.

(Spec., page 8, lines 7-10, emphasis added.) The emphasized language refers to the clock envelope voltage, which is abbreviated VC_{ENV} in Fig. 4 and elsewhere. As in the example of the

signal envelope voltage, the clock envelope voltage is "used" in the manner detailed in connection with Fig. 4 and can also be generated (i.e., "made") using the conventional envelope detector of Fig. 2 (*See Id.* at page 8, lines 10 and 11).

Applicants' specification thus fully describes and schematically details circuits for making and using a "clock envelope voltage" in support of the claims. The rejections of the claims for failing to enable a "clock envelope voltage" should therefore be withdrawn.

Group Envelope Voltage

Applicants' specification makes many references to a "group envelope voltage," the first of which occurs on page 10 in connection with a discussion of Fig. 6.

> Receiver 50 has **group envelope detection circuitry that is responsive to the collective amplified data signals Dour to indicate a group envelope voltage**. In this example, the group envelope detection circuitry comprises a plurality of individual envelope detectors 54 whose capacitive outputs are connected in common to form **a group envelope voltage signal VG_{ENV}**, In this configuration, the detection circuitry is responsive to peaks in any of data output signals DOUT, and VG_{ENV} generally tracks the most extreme peaks occurring at any moment on any of the data output signals.

(Spec., page 10, lines 18-25, emphasis added.) The emphasized language refers to the group envelope voltage, which is abbreviated VG_{ENV} in Figs. 6, 7, 8, and 10.

Fig. 6 and the related text detail how to "use" a group envelope voltage VG_{ENV} to control the gain of a group of amplifiers 52. Fig. 6, reproduced below, shows the group of envelope detectors 54 that generate a group envelope voltage signal VGENV to control the gain of a group of amplifiers 52 via a feedback component 60.

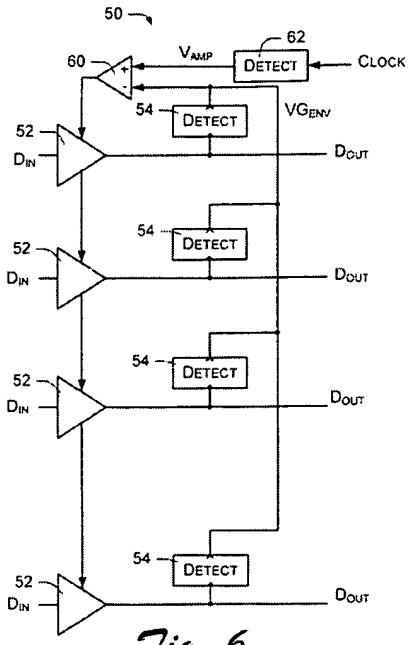

Fig. 6

Figs. 7 and 8, reproduced below, show implementations of group envelope detection circuitry. Each circuit generates, or "makes," a group envelope voltage VG_{ENV} in support of the identical claim language.

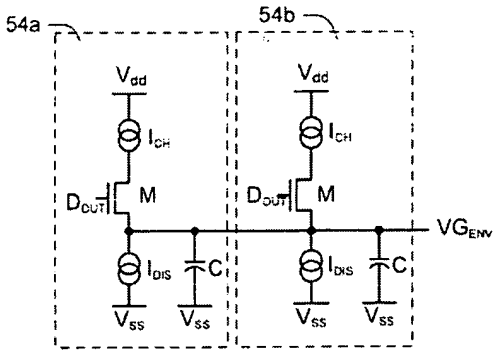

Fig. 7

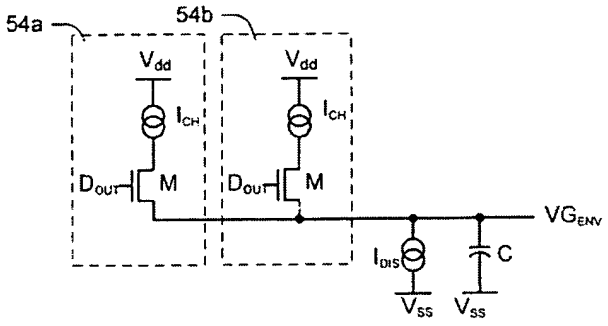

Fig. 8

The manner of making (e.g. Figs. 7 and 8) and using (e.g. Fig. 6) a "group envelope voltage VG_{ENV}" is thus fully described with reference to embodiments detailed in applicants'

specification and figures. The rejections of the claims for failing to enable a "group envelope voltage" should therefore be withdrawn.

CONCLUSIONS

In light of the foregoing remarks and amendments, the pending claims are in condition for allowance; accordingly, applicants' respectfully request a Notice of Allowance. If the examiner's next action is other than the allowance of the pending claims, the Examiner is requested to call applicants' attorney at (925) 621-2113.

Respectfully submitted,

Arthur J. Behiel
Reg. No. 39,603

I hereby certify that this correspondence is being deposited with the United States Postal Service as first-class mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on September 13, 2005.

Laurie Moreno
Name

Signature

In the Figures

Please amend Figs. 11, 13, and 14 as indicated in red ink on the attached sheets. Applicants have also included corresponding substitute sheets, so labeled, for inclusion pending the examiner's approval of the changes. Applicants respectfully request upon approval of these replacement drawing sheets that the Examiner please forward them to the Office of Initial Patent Examination.

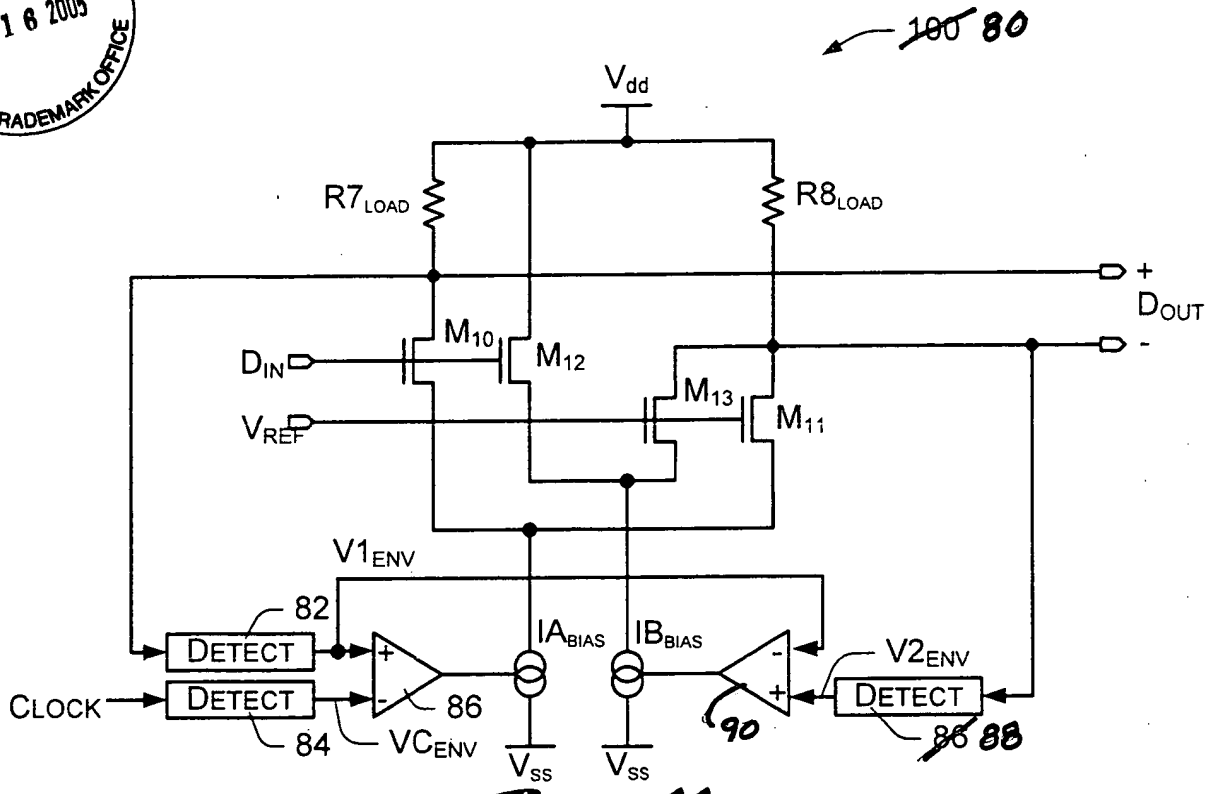

Fig. 11

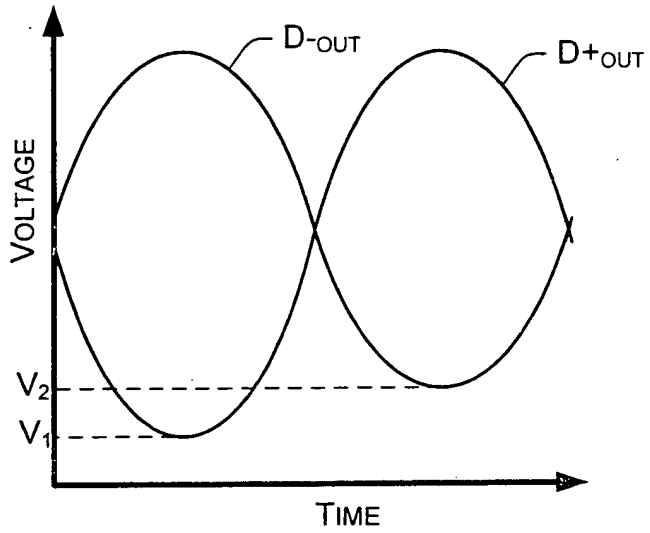

Fig. 12

Prior Art

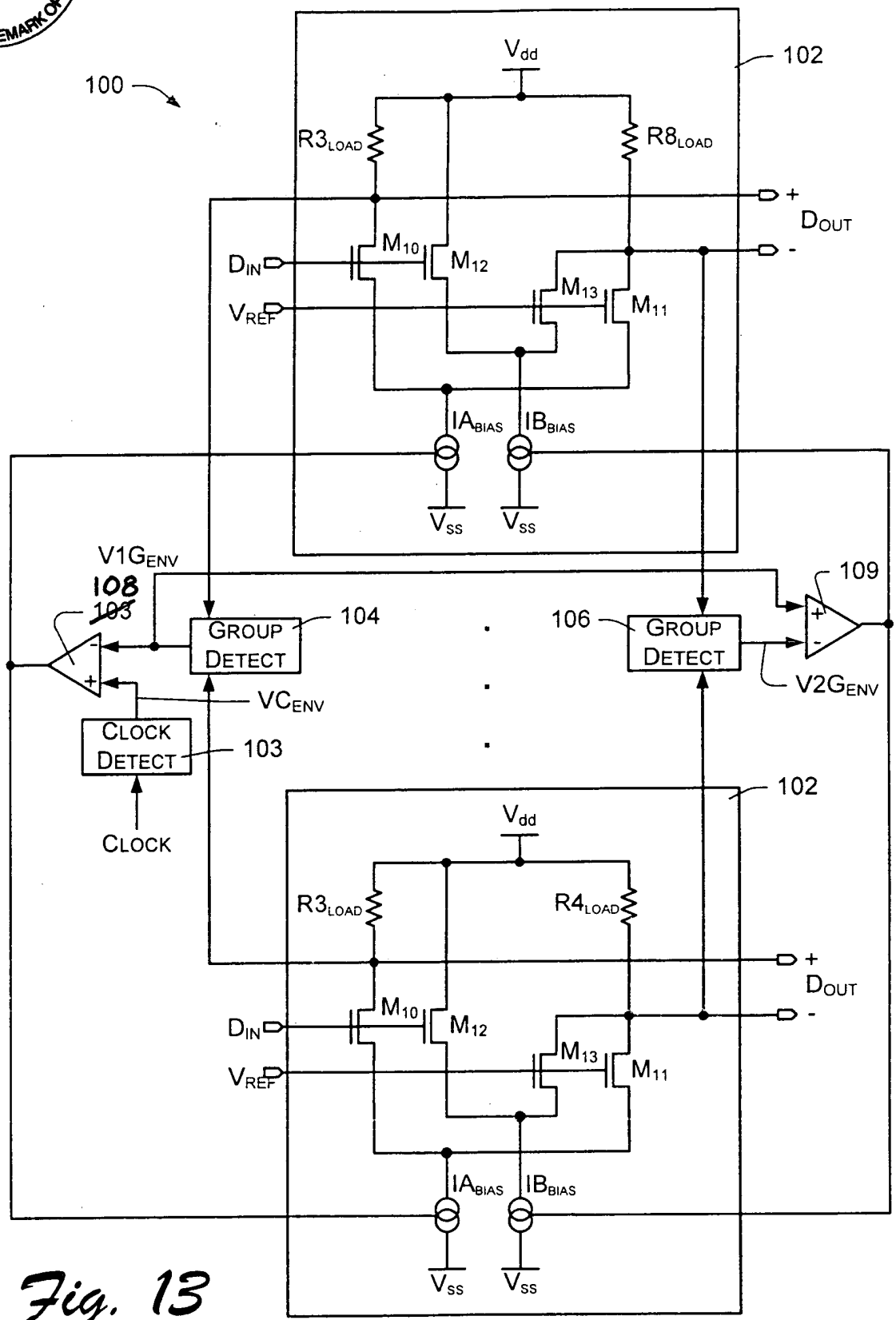

Fig. 13

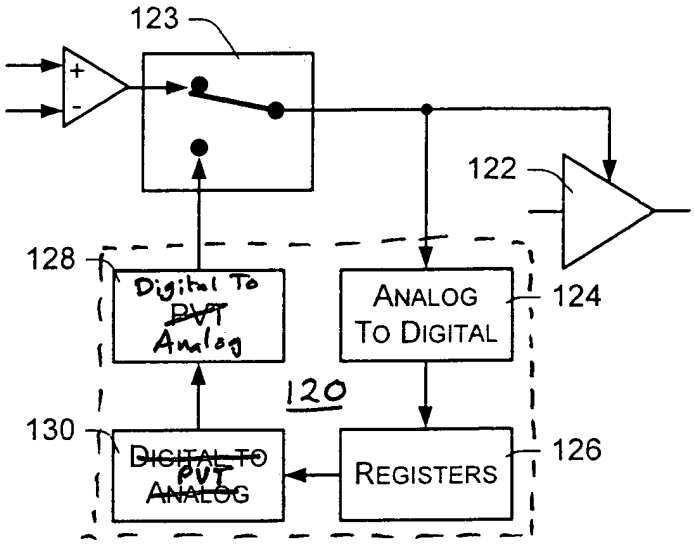

Fig. 14

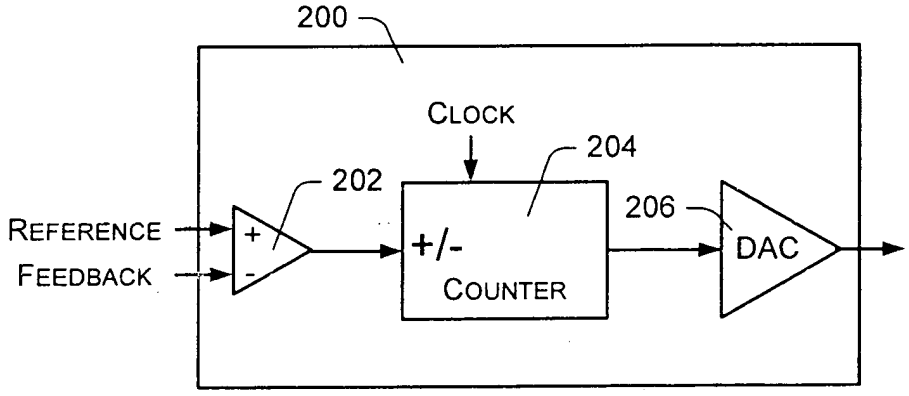

Fig. 15